Amendments to the Claims:

This listing of claims will replace all prior version, and listings of claims in the application:

1-5. (Cancelled)

6. (Currently Amended) A dither code detector receiving a coded signal having a long code composed of a plurality of dithered codes wherein the dithered codes are dithered according to a dither pattern, the detector comprising:

a correlator unit correlating the coded signal with a reference code and outputting a correlation signal;

a detector combining portions of the correlation signal according to the dither pattern and detecting the long code based on the combined portions of the correlation signal,

wherein the detector includes

a delay unit receiving the correlation signal and delaying it according to the dither pattern and outputting delayed correlation signals, and

a combiner receiving the correlation signal and combining it with the delayed correlation signals and outputting a combined correlation signal, and

wherein the delay unit includes

a first counter counting with a first modulus corresponding to a dither of at least a first one of the dithered codes,

a first memory storing a portion of the correlation signal at a location according to a count of the first counter and outputting the portion of the correlation signal when the first counter next addresses the location according to the first modulus, and

wherein the combiner includes an first adder adding a delayed portion of the correlation signal with a current portion of the correlation signal and thereby generating a first combined correlation signal.

7. (Previously Presented) The dither code detector according to claim 6, further comprising a processing unit coupled to the detector and processing the detected long code to determine timing information from the received coded signal.

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) The dither code detector according to ~~claim 9~~ claim 6, wherein the delay unit further comprises:

a second counter counting with a modulus corresponding to a dither of at least a second one of the dithered codes;

a second memory storing a combined correlation signal at a location according to the second counter and outputting the combined correlation signal when the second counter next addresses the location according to the second counter modulus; and

wherein the combiner further comprises a second adder adding a ~~the~~ delayed combined signal with a current portion of the correlation signal and thereby generating a second combined correlation signal.

11. (Previously Presented) The dither code detector according to claim 10, wherein the detector further comprises a maximum finder unit for arranging outputs of the second adder according to the strength of the second combined correlation signal, and if the second combined correlation signal is the largest signal among the signals arranged by the maximum finder, detecting a phase of the long code based on the second combined correlation signal.

12. (Previously Presented) The dither code detector of claim 6, wherein the dither pattern is a stationary dither pattern.

13. (Withdrawn) A maximum finding unit, comprising:

a first storage unit receiving and storing a value of a first signal;

a second storage unit receiving and storing a value of a second signal;

a comparator comparing a value stored in the first storage unit with a current signal value and generating a control signal according to the comparison;

a multiplexer connected to the first and second storage units and the comparator, for arranging the first and second signals in response to the control signal, wherein if the current signal value is greater than the value of the second signal and less than the value of the first signal, then the value of the second signal is moved to a third storage unit and the value of the current signal is stored in the second storage unit.

14. (Withdrawn) The maximum finder unit according to claim 13, wherein the values of the first and second signals are sums of correlation signals formed over a period of a code composed from dithered short codes.

15. (Withdrawn) The maximum finder unit according to claim 14, wherein the dithered short codes are dithered according to a stationary dither pattern.

16. (Currently Amended) A method for detecting a code composed of codes dithered according to a dither pattern, the method comprising:

a) correlating a received signal and a plurality of reference codes thereby generating a plurality of correlation signals;

b) combining the plurality of correlation signals based on the dither pattern and producing a final combined correlation signal, wherein the combining the plurality of correlation signals includes:

b1) delaying a first one of the plurality of correlation signals by an amount equal to the period of a first one of the dithered codes;

b2) adding the delayed correlation signal to a current correlation signal to produce a combined correlation signal;

b3) delaying the combined correlation signal by an amount equal to the period of another one of the dithered codes;

b4) adding the combined correlation signal delayed in b3) to a current correlation signal to produce a new combined correlation signal;

b5) repeating b3) and b4) using delays based on the dither pattern and using the new combined correlation signal in place of the combined correlation signal produced in b2), until the adding of b4) is performed a number of times equal to the number of dithered codes present in the composite code, and then outputting the new combined correlation signal as the final combined correlation signal;

c) detecting the composite code based on the final combined correlation signal.

17. (Previously Presented) The method according to claim 16, further comprising:

d) generating a plurality of combined correlation signals; and

e) arranging the plurality of combined correlation signals in order of the strength of the combined correlation signals.

18. (Cancelled)

19. (Currently Amended) The method according to ~~claim 18~~ claim 16, wherein the delaying of b3) is performed by storing the combined correlation signal in a memory at an address computed modulo N, where N corresponds to the period of said another one of the dithered codes.

20. (Previously Presented) The method according to claim 16, wherein the detecting the composite code includes:

c1) comparing the final combined correlation signal with previously generated final combined correlation signals;

c2) selecting, based on the comparison of c1), the combined correlation signal having the strongest correlation value; and.

c3) detecting the composite code by determining the phase of the long code based on a receive time of the selected combined correlation signal.

21. (Previously Presented) The method according to claim 16, wherein the dither pattern is a stationary dither pattern.